UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,315	06/30/2003	Hiromichi Yamada	83394.0008	4002

26021 7590 01/24/2006

HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
ZALEPA, GEORGE D	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,315	YAMADA ET AL.	
	Examiner	Art Unit	
	George D. Zalepa	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Declaration as filed on 14 October 2003

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 30 June 2003 has been considered by the examiner.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Microcontroller for Decompressing and Compressing Variable Length Codes via a Compressed Code Dictionary.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3-4 and 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Faraboschi et al (US Pat. No. 5,870576; herein referred to as "Faraboschi").

7. Regarding **independent claim 1**,

8. Faraboschi discloses *a micro controller, comprising a CPU* [see Faraboschi, Fig.3, element 230], *performing processing in accordance with a program, said micro controller further comprising: a memory* [see Faraboschi, Fig. 2, element 110], *storing: compressed codes* [see Faraboschi, Fig. 2, element 140], *resulting from the conversion of program codes into variable length codes* [see Faraboschi, Fig. 2, element 140; Col 4, lines 44-46; Examiner's note: With regard to element 140, a first compressed code is represented by memory locations 14000300-14000310, corresponding to the uncompressed codes in cache (100) line 040. A second compressed code corresponds to memory locations 14000314-14000318, corresponding to cache line 041. Both cache lines consist of nine spaces for instructions, however, upon being compressed to memory they are of variable lengths due to the absence or presence of words with in the said nine spaces of a cache line (bundle)]*; an address conversion information, specifying the head address of each group of grouped program codes* [see Faraboschi, Col. 5, lines 2-4; Examiner's note: Faraboschi uses the pointers in element 152 to point to an instruction in the memory which corresponds to the first instruction in a cache bundle, e.g., memory location 14000300 (W00) corresponds to the first instruction in the cache line 040]*; and a compressed code type information, specifying, according to each group, the code length of each compressed code contained in each group* [see Faraboschi, Col. 5, lines 4-5; Examiner's note: Faraboschi utilizes a mask field to record where instructions are located in cache line being examined for compression, this mask records a one (1) for each location that is occupied by an instruction within a cache line. Thus, for line 040 the mask is recorded as "101001110" which indicates that there are five (5) instructions located within cache line 040. This mechanism records how many instructions are within a line (the length) as well as where the instructions are located within the cache line]*; and a compressed code processing part, specifying, from a code address output by the CPU, an*

address conversion information and compressed code type information to be referred [see Faraboschi, Col. 5, 2-5], *using the specified address conversion information and the compressed code type information to determine the corresponding compressed code address* [see Faraboschi, Col. 3, lines 4-14; Examiner's note: Faraboschi, in lines 4-10, uses the code pointer (address conversion information) as described earlier to address the beginning of a compressed code in memory. In lines 10-14, Faraboschi discloses expanding the compressed word to re-create the uncompressed cache line. Faraboschi uses the mask described above to perform this, as stated in Col. 6, lines 26-28], *and reading the corresponding compressed code* [see Faraboschi, Col. 3, lines 11-14].

9. Regarding **claim 3**,

10. Faraboschi discloses *the micro controller as set forth in claim 1, wherein said compressed code processing part stores information for identifying the area in said memory in which compressed codes are stored* [see Faraboschi, Fig. 2, elements 132 and 135], *the area in said memory in which the address conversion information are stored* [see Faraboschi, Fig. 2, element 152], *and the area in which the compressed code type information are stored* [see Faraboschi, Fig. 2, element 150].

11. Regarding **claim 4**,

12. Faraboschi discloses *the micro controller as set forth in claim 3, wherein said memory stores said address conversion information in the order of blocks of program codes* [see Faraboschi, Fig. 2, element 152], *and to store said compressed code type information in the order of the program codes* [see Faraboschi, Fig. 2, element 150; Examiner's note: The table lines (both code pointers (address conversion information and compressed code type) of table 132 correspond to the order in which lines 040-045 of cache 100, thus are in order of program codes].

13. Examiner's note: It is obvious that the data in elements 150 and 152 are in the same program order as the blocks 040-045 as shown by their relationship with the compressed codes ordered in the code heap segment, element 140.

14. Regarding **claim 7**,

15. Faraboschi discloses *the micro controller as set forth in claim 1, wherein said compressed code processing part reads, from said memory and prior to reading a compressed code, a compressed code set, having a predetermined size and containing the compressed code to be read* [see Faraboschi, Col. 6, lines 26-28; lines 47-52; Examiner's note: Faraboschi discloses an entire code set (Fig. 2, element 140, lines 140000300-140000310) into a refill buffer and upon reading the last word, writes said code set into an instruction cache, thus reading a set of compressed words containing a selected compressed code.], *said micro controller is equipped with areas, respectively storing temporarily the address conversion information, the compressed code type information, and the compressed code set that were used just immediately before* [see Faraboschi, Fig. 3, element 100; Examiner's note: The use of the instruction cache is to temporarily hold recently used instructions as described earlier in this paragraph], *to use the address conversion information and the compressed code type information that are stored temporarily in said areas in a case where the code address output by the CPU is contained in the same block as the compressed code that was read just immediately before* [see Faraboschi, Col. 5, lines 61-65; Examiner's note: The purpose of the instruction cache is to speed up the access to instructions that exhibit spatial locality within a compressed code set, thus if an instruction is required that is with in the same code set (i.e., with respect to Fig. 2, accessing instruction W00 after executing instruction W01) the instruction executed immediately after would already be stored within the cache (temporary storage)], *and to read the compressed code from the compressed code set that is stored temporarily in said area in a case where the compressed code corresponding to the code address output by the CPU is contained in the compressed code set that was read just immediately before* [see Faraboschi, Col. 5, lines 64-67].

16. Regarding **claim 8**,

17. Faraboschi discloses *the micro controller as set forth in claim 1, wherein said compressed code contains the same code as the original code* [see Faraboschi, Col. 4, lines 59-62; Examiner's note: It is

obvious as shown in Fig. 3, elements 140 and 040-044 that the same instructions in the uncompressed program (040-044) are the same instructions in the compressed program (140)].

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 2, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraboschi in view of Henkel et al (US Pat. No. 6,691,305; herein referred to as "Henkel").

20. Regarding **claim 2**,

21. Faraboschi discloses the limitations as stated in **independent claim 1**.

22. Faraboschi does not disclose a *memory* [storing] *dictionary information for decompressing compressed codes into the original codes and the compressed code processing part refers the dictionary information to decompress the compressed code, which has been read, into the original code.*

23. Henkel does disclose a *memory* [storing] *dictionary information* [see Henkel, Fig. 19, elements 72 and 78; Examiner's note: The decoding table and "fast dictionary" disclosed by Henkel perform similar functions, the speed at which they perform relative to each other is the difference Henkel points out] *for decompressing compressed codes into the original codes* [see Henkel, Col. 15, lines 13-16] *and the compressed code processing part refers the dictionary information to decompress the compressed code, which has been read, into the original code* [see Henkel, Col. 27, lines 4-9].

24. Regarding **claim 5**,

25. Faraboschi and Henkel disclose the limitations as stated in **claim 2**.

26. Henkel also discloses *dictionary information* [being] *stored in areas that are divided according to the code lengths of the corresponding compressed codes* [see Henkel, Fig. 11A, 11D; Col. 28, lines 2-9; Col. 26, lines 63-67; Examiner's note: With regard to the statements in paragraph 24 of this action, the examiner regards elements 72 and 78 of Fig. 19 as two areas of dictionary information, regarding Figs. 11A and 11D, compressed codes are clearly distinguished by code length and length tags "N.B." for Fig. 11A and "100" for Fig. 11D, thus the two areas are distinguished by code length], *and in each area, said dictionary information are stored in the order of the codes of said corresponding compressed codes* [see Henkel, Col. 27, lines 2-5; Col. 27, lines 7-9; Examiner's note: Since the decoding tables are created during the compression of codes, it is assumed they are created (stored) in the order of the code of the corresponding compressed codes].

27. Regarding **claim 6**,

28. Faraboschi and Henkel disclose the limitations as stated in **claim 5**.

29. Henkel also discloses the *compressed code processing part specifying, from the compressed code type information, the area in which the dictionary information to be referred is stored* [see Henkel, Fig. 11A, 11D, with respect to bits 31-29 which determine whether a compressed instruction is routed to the first decoding table or the second], *and, based on the compressed code, specifies the dictionary information to be referred that is contained in the specified area* [see Fig. 11A, 11D, with respect to "encoded instruction" and "index to fast dictionary" which are used to index the decoding tables].

30. Regarding **claims 2, 5,** and **6**,

31. The advantage of using a decoding table or fast dictionary would have been to increase the speed of decompression by allowing the compressed codes to be decompressed in as few clock cycles as possible. This advantage would have motivated one of ordinary skill in the art at the time of invention to utilize a dictionary lookup concept as disclosed by Henkel within the environment of Faraboschi to eliminate the penalty of accessing an external memory to retrieve all codes. Therefore, it would have

been obvious to one of ordinary skill in the art at the time of invention to add a dictionary look up to the invention disclosed by Faraboschi with the goal of increasing the speed of decompression.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George D. Zalepa whose telephone number is (571) 272-6754. The examiner can normally be reached on Monday-Friday (alt. Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

***

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100